Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (cancel)

Claim 2 (previously presented): The method of claim 17, wherein generating a low-frequency clock further comprises generating an asymmetrical clock signal.

Claim 3 (previously presented): The method of claim 17, further comprising changing the duty cycle by changing a position of the falling edge of a square wave clock relative to a position of the rising edge of the square wave clock.

Claim 4 (previously presented): The method of claim 17, further comprising minimizing an nth-order harmonic associated with the low frequency clock signal.

Claim 5 (previously presented): The method of claim 17, further comprising applying the low frequency clock signal in a digital receiver.

Claims 6-10 (cancel)

Claim 11 (currently amended): A clock generator, comprising:

a high frequency clock/oscillator of a wireless receiver having radio frequency circuitry and baseband circuitry;

a counter coupled to the clock/oscillator; and

a controller coupled to receive an output of the counter to generate a low frequency clock with an asymmetrical duty cycle.

Claim 12 (currently amended): The clock generator of claim 11, wherein the ~~clock oscillator~~ clock/oscillator generates an output at a high frequency relative to the low frequency clock.

Claim 13 (original): The clock generator of claim 11, wherein the counter is a down counter.

Claim 14 (original): The clock generator of claim 11, wherein the counter is a modulo counter.

Claim 15 (previously presented): The clock generator of claim 11, wherein the controller to change the position of a falling edge of a symmetrical clock relative to the position of a rising edge of the symmetrical clock to obtain the asymmetrical duty cycle.

Claim 16 (currently amended): The clock generator of claim 11, wherein the controller to minimize the nth-order harmonic and change the magnitude of other harmonic at a mixer of the wireless receiver.

Claim 17 (currently amended): A method comprising:

obtaining a high frequency clock signal in a wireless transceiver having a predetermined duty cycle; and

generating a low frequency clock signal from the high frequency clock signal at a changed duty cycle to reduce a harmonic of the high frequency clock signal in the wireless transceiver.

Claim 18 (previously presented): The method of claim 17, further comprising changing the predetermined duty cycle based on a count value.

Claim 19 (currently amended): The method of claim 18, further comprising triggering a falling edge of the low frequency clock signal when the count value is ~~below~~ above a threshold.

Claim 20 (currently amended): An apparatus comprising:

an oscillator to generate a first clock signal with a first duty cycle at a first frequency;

a counter coupled to the oscillator; and

a controller to generate a second clock signal at the first frequency with a second duty cycle formed by a first transition and a second transition, the second transition initiated when a value of the counter is at a predetermined value.

Claim 21 (previously presented): The apparatus of claim 20, wherein the oscillator is at an intermediate frequency.

Claim 22 (previously presented): The apparatus of claim 20, further comprising a digital portion.

Claim 23 (previously presented): The apparatus of claim 22, wherein the oscillator and the digital portion are on a single substrate.

Claim 24 (previously presented): The apparatus of claim 23, wherein the second clock signal to be provided to the digital portion.

Claim 25 (new): The clock generator of claim 16, wherein the mixer and the clock/oscillator are on a single integrated circuit.

Claim 26 (new): The clock generator of claim 11, wherein the counter is coupled to receive a first count value and a second count value to set the asymmetrical duty cycle.

Claim 27 (new): The apparatus of claim 20, wherein the counter is coupled to receive a first count value and a second count value to set the second duty cycle.